METHOD AND CIRCUIT CONFIGURATION FOR MULTIPLE CHARGE RECYCLING DURING REFRESH OPERATIONS IN A DRAM DEVICE

ABSTRACT

Methods and circuit configurations for multiple recycling of charge during a refresh operation in a memory device, such as a dynamic random access memory (DRAM) device, are provided. Charge from one or more power lines of a first array of bit line sense amplifiers involved in a first refresh operation may be transferred to one or more power lines of at least second and third arrays of bit line sense amplifiers involved in subsequent refresh operations.